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for

A Method and Apparatus for Improving Stability of a 6T CMOS SRAM Cell

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BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

[0001] The present invention relates to the field of semiconductor integrated circuit design and manufacturing, and more specifically to a 6T CMOS SRAM cell using tri-gate fully depleted substrate transistors and its methods of fabrication.

2. DISCUSSION OF RELATED ART

[0002] As silicon technology continues to scale from one generation to the next, the impact of intrinsic threshold voltage (Vt) variations in minimum geometry size bulk planar transistors reduces the CMOS SRAM cell static noise margin (SNM). This reduction in SNM caused by increasingly smaller transistor geometries is undesirable. SNM is further reduced when Vcc is scaled to a lower voltage.

[0003] Threshold voltage (Vt) variations in planar transistors arise mostly from the statistical fluctuation of the number and/or location of the dopant atoms in the depletion region of the transistors. The Vt variations pose barriers to the scaling of supply voltage, transistor size, and, hence, the minimum six transistor (6T) CMOS SRAM cell size. This limits the total transistor count for conventional 6T SRAM-dominated high performance CMOS ASICs and microprocessors due to die size and cost constraints.

[0004] Currently, the problem of reduced SNM resulting from Vt instability of the SRAM cell transistors is solved at the circuit/layout level by either (a) increasing the minimum supply voltage (Vccmin) needed to operate the cell and keeping the minimum geometry size transistors or (b) increasing the channel length and width of the cell transistors to enable a lower minimum operating voltage at the expense of the minimum cell size. At the device level, in planar devices, Vt mismatch arising from random dopant fluctuations

(RDF) can be minimized by box-shaped wells or super-steep retrograde wells at the expense of additional fabrication process complexity.

[0005] A 6T CMOS SRAM cell circuit diagram using planar transistors is illustrated in Figure 1. The SRAM cell consists of two N-type access devices **102**, two N-type pull-down devices **104**, and two P-type pull-up devices **106**.

[0006] Figure 2 illustrates a 6T CMOS SRAM cell layout using planar transistors. The gate of each access device is located in region **202**. The gate of each pull-down device is located in region **204**. The gate of each pull-up device is located in region **206**. The gate regions are indicated by a region of polysilicon **214** over a region of P-type diffusion **212** or N-type diffusion **210**. Metal layers **218** provide power (Vcc) and ground (Vss). Metal layers **218** may also connect the gate/source/drain of one planar transistor in the cell to the gate/source/drain of another transistor in the cell, and may interconnect one cell to another. Contacts **216** indicate regions where connections may be made to the metal layers. For a given Vcc, the cell ratio is tailored by sizing each access transistor width and each pull-down transistor width to achieve the maximum SNM value.

[0007] Figure 3 is a graph **300** which illustrates the impact of supply voltage scaling on a typical 6T CMOS SRAM cell using planar transistors. The noise margin values assume nominal threshold voltage, nominal Vcc, and nominal device sizes. Dashed line **310** indicates the minimum desired value for SNM, 240 mV. The graph shows that as Vcc scales down from 2V to less than 1V, the cell ratio must increase in order to maintain a desirable SNM value. For a cell ratio of 1.5 **(302)**, the minimum voltage that can be achieved while maintaining a nominal SNM of 240mV is slightly less than 2.0V. When the cell ratio is increased to 2.0 **(304)**, the minimum voltage that can be achieved while maintaining a nominal SNM is less than 1.5V. If the cell ratio is increased to 3.5 **(306)**, the minimum voltage may be reduced to less than 1.0V. However, increasing the cell ratio corresponds to an area penalty in the form of increasing cell size.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Figure 1 is an illustration of a prior art 6T CMOS SRAM cell circuit diagram using planar transistors.

[0009] Figure 2 is an illustration of a prior art 6T CMOS SRAM cell layout using planar transistors.

[0010] Figure 3 is a graph which illustrates Static Noise Margin as a function of Supply Voltage for a 6T SRAM cell of varying cell ratios.

[0011] Figure 4 is a cross-sectional view of a single-fin tri-gate transistor.

[0012] Figure 5 is a cross-sectional view of a dual fin tri-gate transistor.

[0013] Figure 6 is an illustration of a 6T CMOS SRAM cell circuit diagram with tri-gate transistors according to one embodiment of the present invention.

[0014] Figure 7 is an illustration of a 6T CMOS SRAM cell layout using single and dual fin tri-gate transistor according to one embodiment of the present invention.

[0015] Figure 8 is a comparison of the gate width of a dual fin tri-gate transistor according to one embodiment of the present invention and a planar transistor.

[0016] Figure 9 is a graph which compares SNM as a function of supply voltage for a tri-gate SRAM according to one embodiment of the present invention and for a planar SRAM, where both SRAM cells have the same layout area.

[0017] Figure 10 is a flowchart which describes the steps in forming a dual fin tri-gate transistor according to one embodiment of the present invention.

[0018] Figures 11A – 11J illustrate the formation of a dual fin tri-gate transistor according to one embodiment of the present invention.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

[0019] The present invention is a 6T CMOS SRAM cell using non-planar tri-gate transistors, and its method of fabrication. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. In other instances, well-known semiconductor process and manufacturing techniques have not been described in particular detail in order to not unnecessarily obscure the present invention.

[0020] The present invention takes advantage of the higher drive current performance of non-planar tri-gate transistors to improve the stability of the 6T CMOS SRAM cell, thus enabling lower supply voltage operation and reduced cell layout sizes. Tri-gate transistors in multiple fin configurations can deliver more drive current for a given layout width than a planar transistor.

[0021] Figure 4 illustrates a cross section of a typical single fin tri-gate transistor **400**. A single fin tri-gate transistor is a tri-gate transistor having a single semiconductor body **410**. The semiconductor body will also be referred to as a "semiconductor fin." The semiconductor body is formed on an insulating substrate **402**. The insulating substrate is comprised of a buried oxide or other insulating layer **406** over a silicon or other semiconductor substrate **404**. A gate dielectric **416** is formed over the top and on the sides of the semiconductor fin **410**. A gate electrode **420** is formed over the top and on the sides of the gate dielectric. The gate electrode has a gate length $\mathbf{G_L}$. The source, **S**, and drain, **D**, regions are formed in the semiconductor fin on either side of the gate electrode.

[0022] The semiconductor fin has a top surface **412** and laterally opposite sidewalls **414**. The semiconductor fin has a height or thickness equal to **Tsi**. The semiconductor fin has a width equal to **Wsi**. The gate width of a single fin tri-gate transistor is equal to the sum of the gate widths of each of the three gates formed on the semiconductor body, or, **Tsi + Wsi + Tsi**.

[0023] Figure 5 illustrates a cross section of a typical dual fin tri-gate transistor, **500**, according to one embodiment of the present invention. A dual fin tri-gate transistor is a

tri-gate transistor having two semiconductor bodies, or fins, **410** over an insulating substrate **402**, the two fins each having a gate dielectric formed on the top surface and laterally opposite sidewalls, and sharing a single gate electrode formed over and around the gate dielectric. Each semiconductor fin has a top surface **412** and laterally opposite sidewalls **414**. The semiconductor fins are separated by a distance **Ds**. Patterning with normal lithographic techniques allows a minimum **Ds** of approximately 240nm. The gate width of a dual fin tri-gate transistor is equal to the sum of the gate widths for each of the two semiconductor bodies, or [2(Tsi1) + (Wsi1)] + [2(Tsi2) + (Wsi2)]. If the semiconductor bodies are formed in such a way that each semiconductor body has substantially similar dimensions, the gate width of a dual fin tri-gate transistor is effectively twice the gate width of a single fin tri-gate transistor. The gate width of a tri-gate transistor can be further increased by adding additional fins to the tri-gate transistor. A tri-gate transistor in a multiple fin configuration can deliver more drive current for a given layout width than a planar transistor because a tri-gate transistor having the same size as a planar transistor will have a larger gate width.

[0024] Figure 6 illustrates a 6T CMOS SRAM cell circuit diagram using tri-gate transistors according to one embodiment of the present invention. The SRAM cell consists of two N-type access devices, **602**, two N-type pull-down devices, **604**, and two P-type pull-up devices, **606**. Each of the N-type access devices **602** is a single fin tri-gate transistor. Each of the P-type pull-up devices **606** is a single fin tri-gate transistor. Each of the N-type pull-down devices **604** is a dual fin tri-gate transistor. Using a dual fin tri-gate transistor as the pull-down device allows a circuit designer to achieve a higher cell ratio for the SRAM cell. The dual fin tri-gate transistor will deliver more current than the single fin tri-gate transistors, thus increasing the cell ratio without increasing the cell layout size.

[0025] The cell ratio of an SRAM cell is defined as the ratio of the transconductance factor of the pull-down N-type transistor to the transconductance factor of the access N-type transistor. The transconductance factor of a transistor is equal to the ratio of gate width to gate length times the mobility and gate capacitance. Where mobility and gate capacitance

are constant across the access and pull-down transistors, the transconductance factor becomes the ratio of the transistor gate width to the transistor gate length. The transconductance factor of the dual fin tri-gate transistor will be greater than that of the planar transistor, because the transistor gate width of the dual fin tri-gate transistor is greater that of the planar transistor, within the same layout area. Furthermore, the transconductance factor of the dual fin tri-gate transistor will be greater than that of the single fin tri-gate transistor because the ratio of gate width to gate length for the dual fin device will be greater than that of the single fin device. Using a dual fin tri-gate transistor as the pull-down device increases the transconductance factor of the pull-down device, thus increasing the cell ratio of the SRAM cell. As described above, higher, and thus more desirable static noise margin (SNM) levels can be achieved by increasing the cell ratio. The use of non-planar tri-gate transistors in the design of an SRAM cell allows the cell ratio to be increased without increasing the physical cell layout size. Table 1, below, is a comparison of cell ratios for an SRAM cell using planar transistors and an SRAM cell using tri-gate transistors, where each of the SRAM cells has the same layout area.

	Transistor	Transconductance
Planar SRAM Cell* Cell Ratio = 1.5	Pull Down	1.6
	Access	1.1
	Pull Up	1.3
Tri-gate SRAM Cell* Cell Ratio = 2.15	Pull Down	6.0
	Access	2.8
	Pull Up	3.0
*Note: Cell layout areas are the same for each cell		

Table 1

[0026] Figure 7 illustrates a 6T CMOS SRAM cell layout using tri-gate transistors according to one embodiment of the present invention. The gate of each access device is located in region **702**. The gate of each pull-down device is located in region **704**. Each of the pull-down devices is a dual fin device. Each fin of the device is indicated by region **708** on either side of sacrificial block **709**. Sacrificial block **709** is used to form the fins in close proximity to one another. The use of sacrificial block **709** allows the fins to be spaced less than 100nm from one another, which would not be possible using traditional lithography. The gate of each pull-up device is located in region **706**. The gate regions are indicated by a region of polysilicon **714** over a region of P-type diffusion **712** or N-type diffusion **710**. Metal layers **718** provide power (Vcc) and ground (Vss). Metal layers **718** may also connect the gate/source/drain of one planar transistor in the cell to the gate/source/drain of another transistor in the cell, and may connect one SRAM cell to another. Contacts **716** indicate regions where connections may be made to the metal layers. For a given Vcc, the cell ratio is tailored by sizing the gate width of each access transistor and each pull-down transistor to achieve the maximum SNM value. As described above, using an N-type dual fin tri-gate device as the pull-down device and an N-type single fin tri-gate device as the access device allows tri-gate SRAM cell to be designed having a higher cell ratio in the same layout area as a planar SRAM cell.

[0027] Figure 8 is a comparison of the gate width of a dual fin tri-gate transistor according to one embodiment of the present invention to the gate width of a planar transistor in the same layout area. Cross-section **800** shows a dual fin tri-gate transistor formed on an insulating substrate **808**. The fins of the tri-gate transistor are formed by semiconductor bodies **802**. The fins are separated by a distance, **Ds**, which is determined by the width of the sacrificial block described above. The distance, **Ds**, may be defined by the minimum lithography feature size that may be patterned. A gate dielectric **804** covers each fin of the tri-gate transistor in the gate region. Gate electrode **806** is formed over and around each semiconductor fin and gate dielectric layer. Three gates, **G1**, **G2**, and **G3** are formed for each fin of the dual fin tri-gate transistor. Each gate formed has a gate width. The gate width of **G1** is equal to **Z1**, or the height of the fin. The gate width of **G2** is equal to **Z2**, or the width of the fin. The gate width of **G3** is equal to **Z3**, or the height of the fin. The total gate width of each fin is equal to **Z1 + Z2 + Z3**. For a dual fin tri-gate transistor, the total gate width is equal to **2(Z1 + Z2 + Z3)**. A tri-gate transistor having N fins has a total gate width equal to **N(Z1 + Z2 + Z3)**. In one embodiment of the present invention, Z1 = 60nm, Z2 = 60nm, Z3 = 60nm, and D_s = 60nm. The gate width of the tri-gate transistor according to this embodiment is 2(60nm + 60nm + 60nm), or 360nm. The total layout width used is equal to Z3 + D_s + Z3, or (60nm + 60nm + 60nm) = 180nm.

[0028] Cross-section **820** shows a planar transistor formed on a semiconductor substrate **828**. The gate width of the planar transistor is equal to the width of transistor gate **822**, or **Zp**. For a layout width of 180nm, the gate width of planar transistor **820** is equal to 180nm. Because the gate width of the tri-gate transistor is two times that of the planar transistor for the same layout area, it is possible to increase the cell ratio of a 6T CMOS SRAM cell by designing the cell using single and dual fin tri-gate transistors according to one embodiment of the present invention.

[0029] Figure 9 is a graph **900** which illustrates static noise margin (SNM) as a function of VCC for a planar SRAM cell **920** and a tri-gate SRAM cell **910**, where the cells are the same size. A tri-gate SRAM cell design allows for lower scaling of VCC before exceeding a lower

SNM limit of 240mV (**930**). Because the cell ratio is higher when the SRAM cell is designed using tri-gate transistors according to one embodiment of the present invention, the supply voltage can be scaled lower without reducing the SNM below 240mV. An SRAM cell designed using planar transistors can be operated at a supply voltage of slightly less than 2.0V without reducing the SNM to less than 240mV. An SRAM cell of the same size, but designed using dual and single fin tri-gate transistors according to one embodiment of the present invention, may be operated at a much lower supply voltage before the SNM limit is met. The supply voltage may be as low as 1.25V before the SNM is reduced to less than 240mV.

[0030] Figure 10 is a flow diagram, **1000**, showing a process in accordance with the present invention, illustrating a general method for forming a multiple fin tri-gate transistor having a reduced layout width. Each block in flow diagram **1000** is illustrated and described in further detail below, in conjunction with figures 11A-11J.

[0031] A silicon or semiconductor film is formed on an insulating substrate, as described in block **1002**. The insulating substrate includes a lower monocrystalline silicon substrate and a top insulating layer, such as a silicon dioxide film or a silicon nitride film. The insulating layer is sometimes referred to as a "buried oxide" layer. In one embodiment of the present invention, the semiconductor film has a thickness of 60 nm.

[0032] A sacrificial block having a top surface and laterally opposite sidewalls is then formed on the semiconductor film, as described in block **1004**. In one embodiment of the present invention, the sacrificial block is formed by first forming a layer of the sacrificial material and patterning the sacrificial material to form a block using lithography. The sacrificial block may be comprised of nitride, but is not limited to nitride. The width of the sacrificial block determines the spacing of the fins. In one embodiment of the present invention, the laterally opposite sidewalls of the sacrificial block are 60nm apart. In another embodiment of the present invention, the laterally opposite sidewalls of the sacrificial block are separated by a distance defined by the minimum feature size that may be formed using lithography.

[0033] After forming the sacrificial block, an insulating layer is formed over and around the sacrificial block and the semiconductor film, as described in block **1006**. The insulating layer may be comprised of an oxide or another insulating material. The insulating layer is deposited such that the thickness of the layer is approximately equal to the desired semiconductor fin width. In one embodiment of the present invention, the thickness of the insulating layer is between 40 and 80nm. In another embodiment of the present invention, the thickness of the insulating layer is 60nm.

[0034] Insulating spacers are then formed on either side of the sacrificial block by performing an anisotropic etch on the insulating layer, as described in block **1008**. After the anisotropic etch, insulating spacers will remain on either side of the sacrificial block. The width of the insulating spacers will be equal to the thickness of the original insulating layer. In one embodiment of the present invention, the insulating spacers are 60nm wide.

[0035] In another embodiment of the present invention, multiple sacrificial blocks may be formed, to form additional spacers. This method may be used to form a tri-gate transistor having more than two fins. The number of fins formed will be equal to the number of insulating spacers. In one embodiment of the present invention, an even number of fins (2N) may be formed. To form a tri-gate transistor having 2N fins, N sacrificial blocks and 2N insulating spacers are required.

[0036] After the insulating spacers are formed, the sacrificial block may be removed by conventional methods, as shown in block **1010**. For example, a selective etch process may be used to remove the sacrificial block, while the insulating spacers remain intact.

[0037] Next, two semiconductor fins are formed by etching the semiconductor film using the insulating spacers as a mask, as shown in block **1012**. The semiconductor film is etched away in areas not covered by the insulating spacers, exposing the insulating substrate. Each semiconductor fin formed has a top surface and a pair of laterally opposite sidewalls. Using the insulating spacers as a mask allows the fins to be separated by a distance that is less than the distance that could be achieved using current lithographic technology. Current lithography allows printing of features having minimum sizes near 60nm and

minimum spacing between features of near 240nm. Using an embodiment of a method according to the present invention, the fins can be formed less than 240nm apart. In one embodiment of the present invention, the fins are separated by a distance of 60nm or less.

[0038] Figures 11A through 11J illustrate the formation of a dual fin tri-gate transistor according to one embodiment of the present invention. The fabrication of a dual fin tri-gate transistor begins with an insulating substrate **1102**, as shown in Figure 11A. A silicon or semiconductor film **1108** is formed on insulating substrate **1102**. Insulating substrate **1102** may be comprised of a lower monocrystalline silicon substrate **1104** and a top insulating layer **1106**, such as a silicon dioxide or silicon nitride film. Insulating layer **1106** isolates semiconductor film **1108** from substrate **1104**, and is sometimes referred to as a "buried oxide" layer. Semiconductor film **1108** may be comprised of silicon or another semiconductor, such as but not limited to germanium (Ge), a silicon-germanium alloy (Si_xGe_y), gallium arsenide (GaAs), InSb, GaP, GaSb, or carbon nanotubes. The semiconductor film **1108** may be an intrinsic, or undoped, silicon film, or it may be doped to a p-type or n-type conductivity. The semiconductor film **1108** is formed to a thickness, **Tsi**, which is approximately equal to the height desired for the subsequently formed semiconductor fins of the tri-gate transistor. In one embodiment of the present invention, the semiconductor film **1108** has a thickness of 60nm or less.

[0039] Figure 11B illustrates the formation of a sacrificial block on the top surface of semiconductor film **1108**. The sacrificial block may be formed by conventional semiconductor manufacturing techniques, including but not limited to depositing a layer of the sacrificial material, **1109**, and subsequently patterning the layer with resist **1111**. The sacrificial material that is not covered by resist **1111** may be etched to form one or more sacrificial blocks in the desired location(s). In one embodiment of the present invention, the sacrificial material **1109** is comprised of a nitride. The width of the sacrificial block to be formed, **Ws**, will define the subsequent spacing of the semiconductor fins of the tri-gate transistor. In one embodiment of the present invention, **Ws** is 60nm or less. The use of a sacrificial block allows the semiconductor fins to be separated by distances of 60nm or less,

which is significantly less than the distance between features that can be achieved by conventional lithography techniques.

[0040] Figure 11C illustrates the formation of an insulating layer **1112** over and around the insulating block **1110** and over the surface of the semiconductor film **1108**. In one embodiment of the present invention, the insulating layer is comprised of an oxide. The insulating layer **1112** is deposited in a manner which allows the layer to have a uniform thickness, **Tox**. The thickness of the insulating layer will determine the width of the semiconductor fins in a subsequent processing step. In one embodiment of the present invention, the insulating layer has a thickness of 60nm or less.

[0041] Figure 11D illustrates the formation of insulating spacers **1114**. Insulating spacers **1114** are formed by performing an anisotropic etch on the insulating layer **1112** of Figure 11C. The anisotropic etch is performed in a manner that allows the insulating layer to be entirely removed from the top surface of the sacrificial block **1110**, but leaves insulating spacers **1114** on either side of the sacrificial block. The insulating spacers **1114** are formed having a width, **Wox**, which is equal to the thickness of the insulating film of Figure 11C, **Tox**. In one embodiment of the present invention, the width, **Wox**, of each insulating spacer is 60nm or less.

[0042] Figure 11E illustrates the structure formed after the removal of the sacrificial block. The sacrificial block may be removed by conventional methods, including the use of a selective etch process. For example, a wet etch may be used to remove a sacrificial nitride block, while the oxide spacers will remain unaffected by the etch process. After the sacrificial block is removed, two insulating spacers **1114** remain, each spacer having a width equal to **Wox**. The spacers are separated by a distance equal to the width of the sacrificial block, **Ws**.

[0043] Figure 11F illustrates the formation of semiconductor fins **1120**. Semiconductor fins **1120** are formed by etching semiconductor film **1108** using insulating spacers **1114** as a mask. In one embodiment of the present invention, the etch is a plasma dry etch process. The semiconductor film is etched completely, exposing the surface of insulating substrate

1102. The semiconductor fins are formed having a width, **Wsi**, which is equal to the width of the insulating spacers used as a mask. In one embodiment of the present invention, **Wsi** is 60nm or less. The semiconductor fins are separated by a distance, **Ds**, which is equal to the width of the sacrificial block formed previously. In one embodiment of the present invention, **Ds** is 60nm or less.

[0044] After the semiconductor fins **1120** are formed, the insulating spacers may be removed by conventional techniques, as illustrated in Figure 11G. At this point, two semiconductor fins **1120** remain on the insulating substrate **1102**. The semiconductor fins **1120** have a top surface, **1121**, and laterally opposite sidewalls, **1123**. The total layout width of the device will be equal to **Wsi + Ds + Wsi**. In one embodiment of the present invention, the total layout width of the device is 180nm or less.

[0045] Figure 11H illustrates the formation of a gate dielectric layer **1122** on the top surface **1121** and on the sidewalls **1123** of each semiconductor fin **1120**. The tri-gate transistor can be designed to be inherently immune from Vt instability by careful control over the geometry of the corners **1125** of the semiconductor fin. The corner of the semiconductor fin is formed by the intersection of adjacent gates, **G1**, **G2**, and **G3**, (top and side) of the device. Because the corner **1125** of the tri-gate transistor turns on first, it determines the threshold voltage (Vt) of the device. When Vt is set only by dopant implants, there may be fluctuations in the dopants which in turn can cause Vt fluctuations. When corner rounding is controlled, the tri-gate transistor is not dependent on doping to set the Vt, and so the transistor can be designed to be inherently immune from Vt instability. Corner rounding of the silicon fin arises primarily from the gate dielectric formation process. The gate dielectric **1122** may be grown or deposited on the surface and sidewalls of the silicon fin. In one embodiment of the present invention, the gate dielectric layer is deposited using Atomic Layer Deposition (ALD), which allows corner rounding to be controlled to atomic dimensions. In one embodiment of the present invention, the radius of curvature, **R**, of each corner of the semiconductor fin is less than 10nm.

[0046] Next, a gate material is deposited over the top surface and sidewalls of each semiconductor fin and over the insulating substrate, as illustrated in Figure 11I. The gate material is patterned to form a gate electrode **1124** on the gate dielectric layer.

[0047] After the gate electrode is formed, a pair of source/drain regions is formed in each semiconductor fin on opposite sides of the gate electrode, as illustrated in Figure 11J. In one embodiment of the present invention, source and drain regions are formed by implanting N-type or P-type dopants into the semiconductor body, as illustrated by arrows **1130**. In embodiments of the present invention, further operations may be performed on the tri-gate device, including, but not limited to, formation of tip or source/drain extension regions, halo regions, heavily doped source/drain contact regions, silicon deposited on the source/drain and gate electrode regions, and silicide formation on the source/drain and gate electrode regions.

[0048] As illustrated in Figure 11J, each semiconductor fin of the resulting dual fin tri-gate transistor has a gate width that is equal to 2Tsi + Wsi. The gate width for the dual fin tri-gate transistor is equal to the sum of the gate widths for each fin, or 2(2Tsi + Wsi). The device may be manufactured in an area having a layout width of 2Wsi +Ds. In one embodiment of the present invention, the gate width of the dual fin tri-gate transistor is 360nm or less, and the device is formed in an area having a layout width of 180nm or less.

[0049] In other embodiments of the present invention, the method set forth above may be used to form tri-gate transistors having more than two semiconductor fins.